Mainframe hardware course: Mainframe's processors

z/OS Basic Skills: The mainframe's processors

Mainframe's processors

This hardware course introduces you to one model of IBM® mainframe computer, the IBM System z9™, to help you learn about the hardware parts that constitute the mainframe's processor by comparing processing parts and functions to personal computers or notebooks.

Time to complete: 10 - 15 minutes

- The central processor complex
- The multichip module
- Memory cards
- Input/output connections
- The mainframe's processing capacity

The central processor complex

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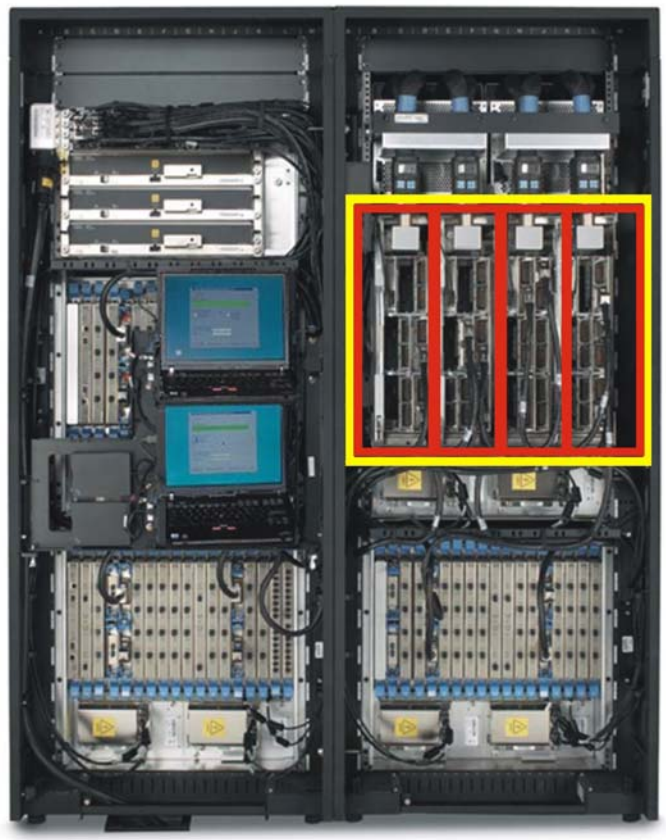
Mainframe's processors > The central processor complex

Mainframes have one or two metal frames that contain specialized cages, as well as other physical elements. This diagram shows the interior front view of an IBM System z9 Enterprise Class (z9 EC) model that has two frames. The z9 EC is slightly larger than a household refrigerator.



The central processor complex, or CPC, resides in its own cage inside the mainframe, and consists of one to four book packages. Just like its personal-computer counterpart, the motherboard or system board, each book package consists of processors, memory, timers, and I/O connections.

These collections of hardware parts are called "book packages" because you can slide them in or out of the CPC cage almost as easily as you can slide a book on or off a bookshelf.

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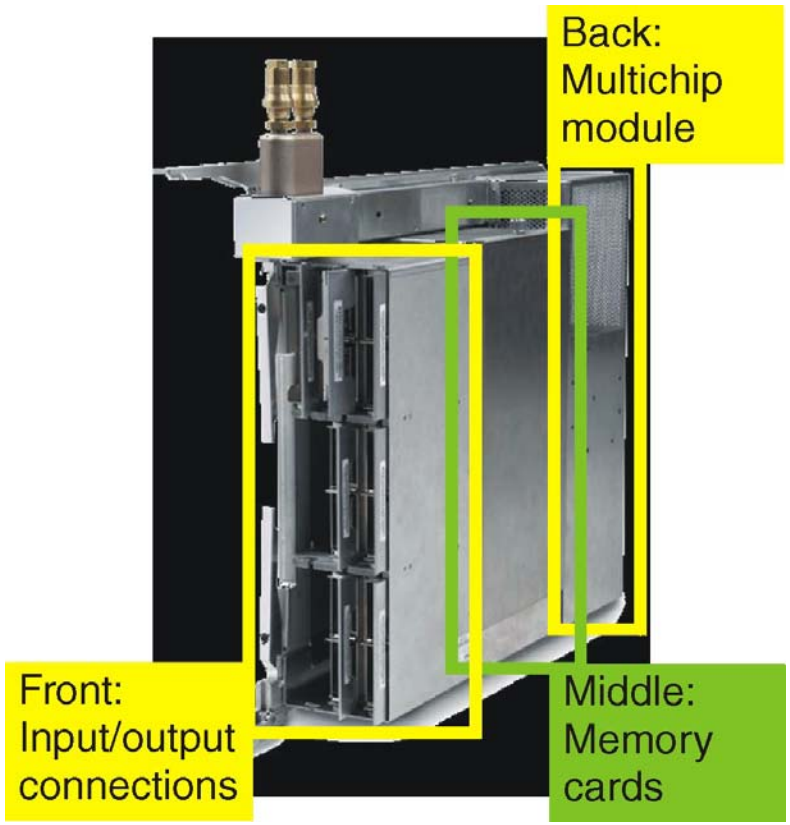
Mainframe's processors > The book package

In the System z9, as well as earlier IBM mainframe models, the book package consists of three distinct areas, one each for:

- The z9 EC's processors, which are inside one multichip module
- Memory cards
- Connections to input/output devices

All of the book packages plug into a backplane in the z9 EC's frame. A backplane is a circuit board that allows all connected book packages to share resources.



The multichip module

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Mainframe's processors > The multichip module

The back of each book package in the central processing complex cage contains one multichip module, or MCM. This module contains 16 complementary metal oxide semiconductors chips, also known as CMOS chips.

CMOS (pronounced *see-moss*) is a widely used technology for manufacturing processors and memory because CMOS chips require less power than other chips that use only one type of transistor. Transistors are tiny devices that switch electrical current on and off.

Mainframe's processors > Multichip module size

The z9 EC multichip module packs the most memory into the smallest logic package used in the computer industry.

Although each module contains 16 CMOS chips, it measures approximately 3.75 by 3.75 inches, or 95 by 95 millimeters. That small space also contains over 100 glass ceramic layers, approximately 0.3 miles (or 545 meters) of internal wiring, and more than 4.5 **billion** transistors.

Mainframe's processors > Chip redundancy

As with other hardware elements in the z9 EC, the multichip module provides built-in redundancy; that is, several chips perform the same function or, although specific chips are reserved for specific functions, another chip can take over for a failing chip.

For example, if the clock chip fails, another chip in the module can assume the function of controlling processor timing. This capability is called dynamic failover, which is a key factor that contributes to the mainframe's continuous availability.

In mainframe models before the z9 EC, a clock failure meant that the mainframe was not available for any work until the damaged clock chip could be replaced. The z9 EC, however, can dynamically switch to another clock chip without losing a beat!

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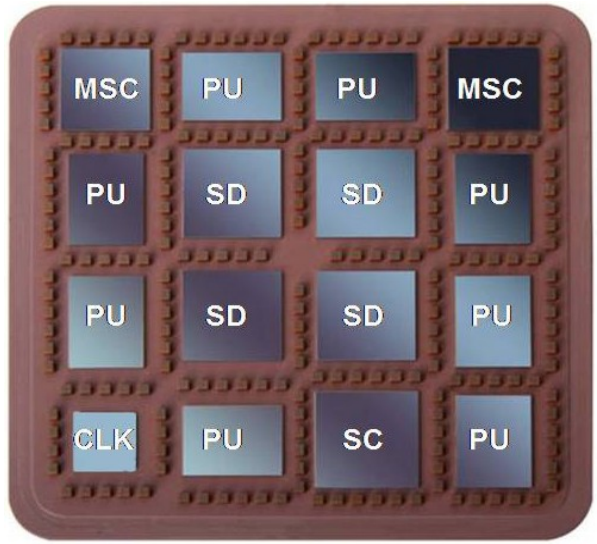
Mainframe's processors > CMOS chip types



Of the 16 CMOS chips in each z9 EC multichip module:

- Four are system data or SD chips containing global memory that all of the z9 EC's configured processors may access. This shared global memory enables the z9 EC's processors to execute program instructions very quickly—in a fraction of one nanosecond!

- One chip is for the storage controller or SC, which controls access to and storage of data in the memory on all of the chips in the book package.

- Two chips are for the memory storage control or MSC subsystem, which handles the transfer of data between processor chips and memory cards in the book package.

- One chip is the oscillator clock, which is abbreviated CLK. The oscillator synchronizes and paces the z9 EC's operations.

- Eight are processor unit or PU chips, which are the workhorses of the z9 EC.

Mainframe's processors > Processor unit chips

Each processor unit chip is designed to provide either one or two physical processor units, and also contains private memory for each processor to store instructions and data.

When a z9 EC is installed, it often has a spare processor; that is, an uncharacterized processor unit chip. If the system controllers detect a failing processor chip, it can be replaced with the spare. In most cases, this switchover can be done without any system interruption, even for the application running on the failing processor.

Alternatively, spare processor unit chips can be enabled at certain times; for example, during unexpected peak workloads. This capability is called capacity on demand.

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Mainframe's processors > General processor characterizations

Each of the eight processor unit or PU chips is characterized by IBM during installation or by customers at a later time. The most common characterizations are:

- **Central processor**, which is abbreviated CP. This type is for use with an operating system and user applications. Mainframe operating systems are sophisticated products with substantially different characteristics and purposes. One mainframe can run more than one operating system at the same. The z9 EC supports these operating systems:
  - z/OS®
  - z/VM®
  - z/VSE™
  - Linux® for zSeries®
  - z/TPF

- **System Assistance Processor**, which is abbreviated SAP. Every mainframe has at least one SAP; larger systems may have several. The SAPs handle input/output subsystem operations; for example, SAPs manage multiple paths to control units and perform error recovery for temporary errors.

Mainframe's processors > Specialized processor characterizations

Each of the eight processor unit or PU chips is characterized by IBM during installation or by customers at a later time. Specialized processor characterizations include:

- **Integrated Facility for Linux**, or IFL. This type helps reduce software costs on the mainframe. It supports new Linux workloads and open standards on the System z platform.

- **System z9 Application Assist Processor**, or zAAP. This type also helps reduce software costs on the mainframe. It supports the same Java™ code that can be run on a standard central processor.

- **System z9 Integrated Information Processor**, or zIIP. This type handles some database-related workloads. The zIIP reinforces the mainframe's role as the data hub of the enterprise by helping to make direct access to DB2 more cost effective and reducing the need for multiple copies of the data.

- **Integrated Coupling Facility**, or ICF. This processor type allows a group of mainframes to share data. A coupling facility is, in effect, a large memory scratch pad used by multiple systems to coordinate work.

Memory cards

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Mainframe's processors > Memory capacity

The middle of each book package in the central processor complex cage contains from four to eight memory cards. Each memory card contains four, eight, or 16 gigabytes of memory.

For memory capacity, a gigabyte is 1 073 741 824 bytes, which is equivalent to the contents of approximately 1 000 lengthy paperback books.

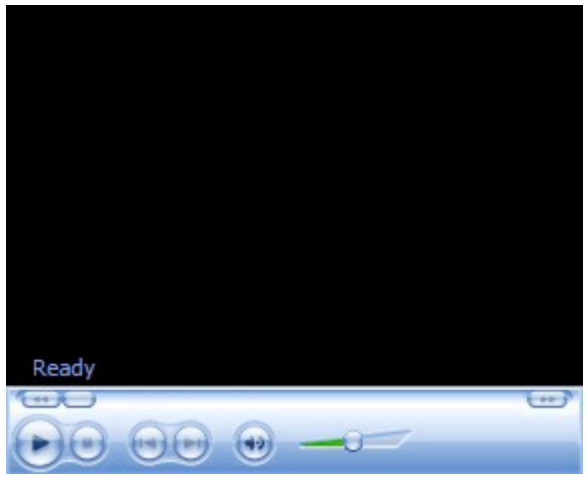
If you do the math, one book package containing the maximum number of eight MCMs can provide up to 128 gigabytes of physical memory; a z9 EC with the maximum number of four book packages can provide up to 512 gigabytes.

Mainframe's processors > Memory card design

Each memory card has two ports, each with a maximum bandwidth of eight gigabytes per second.

The memory cards also are hot-pluggable, or hot-swappable, which means that you can add or remove a memory card without powering down the mainframe.

These memory cards can be used in many of IBM's System i™ and System p™ mainframe and mid-range computers, not just in the System z9 mainframes.



To learn more about the cost and flexibility of memory cards, play this 1-minute video clip featuring Dave Anderson, a hardware expert from IBM's Customer Briefing Center team in Poughkeepsie, New York, where mainframes are designed, manufactured and tested.

Input/output connections

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Mainframe's processors > The mainframe's I/O superhighway

In a personal computer or notebook, the processor is connected to input/output (I/O) devices through a combination of hardware parts: A bus (USB or SCSI, for example), expansion slots, and cables. Personal computers typically have a very limited number of expansion slots for peripheral devices, such as printers, DVD drives, and so on.

The z9 EC has similar hardware parts and connections but the difference in scale is substantial: Comparing PC I/O to mainframe I/O is like comparing a one-lane road to a 10-lane superhighway!

To get a better idea of the mainframe's input/output capacity, just compare the connections for your personal computer to this view of the cables connecting the mainframe to its peripheral devices.

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Mainframe's processors > Parts of the I/O superhighway

The front of each book package in the CPC cage is where the information superhighway starts. Here you find several key hardware parts that connect the z9 EC processors and memory to a myriad of I/O devices.

- Closest to the processors and memory are slots for up to eight memory bus adapter or MBA fanout cards. These cards, along with a specialized processor chip in the z9 EC's multichip module, control the flow of data to and from memory in the book package.

- Each MBA card has two thick self-timed interconnect, or STI, cables that connect the card to the input/output cages in the z9 EC frame. Each cable has a bidirectional bandwidth of 2.7 gigabytes per second. A gigabyte is defined as 1 000 000 000 bytes, which is equivalent to the contents of approximately 1 000 lengthy paperback books.

So a z9 EC with four book packages, each with eight MBA cards and 16 STI cables attached, has a potential instantaneous bandwidth of ***172 gigabytes per second***.

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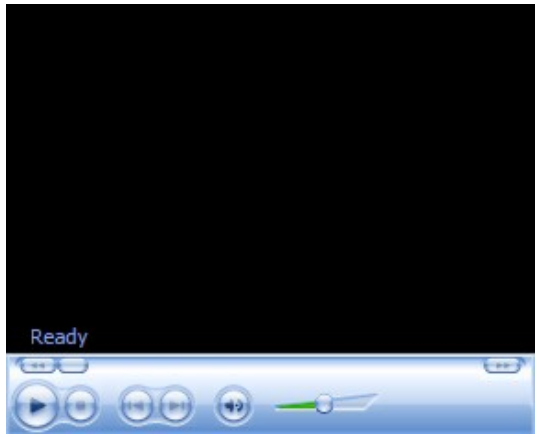
Mainframe's processors > I/O capacity and design



Many hardware parts constitute the high-speed subsystem that provides a path between the mainframe and peripheral devices. The capacity of this subsystem is measured by the number of available channels, which are independent pathways that transfer data. A single z9 EC mainframe can have up to 1 024 individual channels!

The mainframe's high-speed input/output subsystem includes:

- Hardware parts inside and connected to the z9 EC's input/output cages;
- Specialized input/output equipment on the raised floor, such as input/output controllers; and
- The memory bus adapter or MBA cards in the z9 EC's book package, and the self-timed interrupt or STI cables attached to those cards.

To learn more about MBA cards and STI cables, play this 1-minute video clip featuring Dave Anderson, a hardware expert from IBM's Customer Briefing Center team in Poughkeepsie, New York, where mainframes are designed, manufactured and tested.

The mainframe’s processing capacity

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Mainframe’s processors > Scalability and logical partitions

A mainframe’s scalability (that is, its ability to expand resources such as processors, memory, or storage) is measured by the number of system images that the hardware and software are designed to support.

Each system image, or logical partition, is a subset of hardware resources (processors, memory, and input/output devices) defined to support an operating system. This capability—having multiple systems work together as a seamless system—is called virtualization.

Each of these logical partitions, or LPARs, functions as an independent system, just like dual-boot systems on your personal computer. And just as you can have different operating systems boot up on your PC, z9 EC system programmers can configure a different operating system to run on each LPAR.

For example, you might have a PC that runs either Windows® or Linux, but only one of those systems can be running on your PC at a given time. On a z9 EC, several different operating systems (z/OS, Linux, and UNIX®, to name several) can run simultaneously, each on a separate LPAR. While PCs and notebooks have a current limit of four physical partitions and four logical partitions, the z9 EC has many more.

Mainframe's processors > Scalability and processors

In the z9 EC, the number of system images is not necessarily limited to the physical number of processor chips in the mainframe. In fact, each chip is either a single-core or dual-core chip; single-core chips support only one processor, while dual-core chips can support two processors.

Depending on the number of book packages in the CPC cage, a single z9 EC can be logically partitioned into as many as 54 processors (sometimes called "engines") each with the capability of executing 600 million instructions per second (MIPs).

To express these processing and scalability measurements, you often hear people say something like "The z9 EC has a 600-MIP engine that scales up to a 54-way."

Although this characteristic of mainframes is not truly comparable in personal computers, you could say that the z9 EC's scalability is like having multiple Intel® chips in your PC instead of only one chip.

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